500mA Negative Low Dropout Micropower Regulator

FEATURES

- Stable with Wide Range of Output Capacitors
- **Operating Current: 45μA**
- Shutdown Current: 10μA
- **Adjustable Current Limit**
- Positive or Negative Shutdown Logic
- **Low Voltage Linear Dropout Characteristics**
- Fixed 5V and Adjustable Versions
- Tolerates Reverse Output Voltage

APPLICATIONS

- Analog Systems
- Modems
- Instrumentation
- A/D and D/A Converters
- Interface Drivers
- Battery-Powered Systems

DESCRIPTION

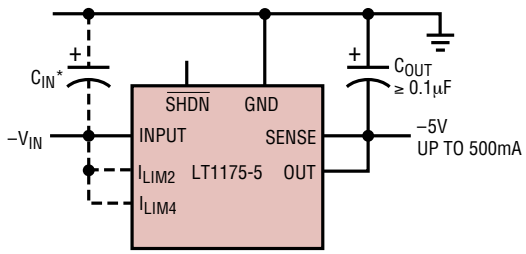
The LT®1175 is a negative micropower low dropout regulator. It features 45μA quiescent current, dropping to 10μA in shutdown. A new reference amplifier topology gives precision DC characteristics along with the ability to maintain good loop stability with an extremely wide range of output capacitors. Very low dropout voltage and high efficiency are obtained with a unique power transistor anti-saturation design. Adjustable and fixed 5V versions are available.

Several new features make the LT1175 very user-friendly. The $\overline{SHDN}$ pin can interface directly to either positive or negative logic levels. Current limit is user-selectable at 200mA, 400mA, 600mA and 800mA. The output can be forced to reverse voltage without damage or latchup. Unlike some earlier designs, the increase in quiescent current during a dropout condition is actively limited.

The LT1175 has complete blowout protection with current limiting, power limiting and thermal shutdown. Special attention was given to the problem of high temperature operation with micropower operating currents, preventing output voltage rise under no-load conditions. The LT1175 is available in 8-pin PDIP and SO packages, 3-lead SOT-223 as well as 5-pin surface mount DD and through-hole TO-220 packages. The 8-pin SO package is specially constructed for low thermal resistance.

TYPICAL APPLICATION

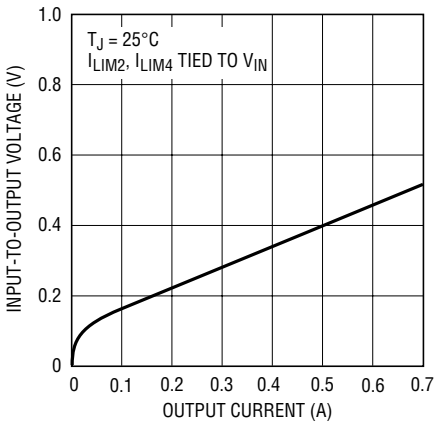
Typical LT1175 Connection



*C_{IN} IS NEEDED ONLY IF REGULATOR IS MORE THAN 6" FROM INPUT SUPPLY CAPACITOR. SEE APPLICATIONS INFORMATION SECTION FOR DETAILS

1175 TA01

Minimum Input-to-Output Voltage

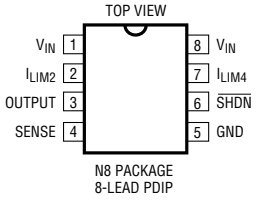


1175 TA02

ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Voltage (Transient 1 sec, Note 11) 25V
Input Voltage (Continuous) 20V
Input-to-Output Differential Voltage (Note 12) 20V
5V SENSE Pin (with Respect to GND Pin) ..... 2V, –10V
ADJ SENSE Pin
(with Respect to OUTPUT Pin) ..... 20V, –0.5V
5V SENSE Pin
(with Respect to OUTPUT Pin) ..... 20V, – 7V
Output Reverse Voltage 2V
$\overline{SHDN}$ Pin to GND Pin Voltage (Note 2) ..... 13.5V, –20V
$\overline{SHDN}$ Pin to V_{IN} Pin Voltage ..... 30V, –5V
Operating Junction Temperature Range
LT1175C ..... 0°C to 125°C
LT1175I ..... –40°C to 125°C
Ambient Operating Temperature Range
LT1175C ..... 0°C to 70°C
LT1175I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

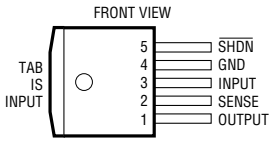


N8 PACKAGE
8-LEAD PDIP

θ_{JA} = 80°C/W TO 120°C/W DEPENDING ON PC BOARD LAYOUT

ORDER PART NUMBER

LT1175CN8
LT1175CN8-5
LT1175IN8
LT1175IN8-5

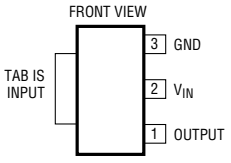


Q PACKAGE
5-LEAD PLASTIC DD

θ_{JA} = 27°C/W TO 60°C/W DEPENDING ON PC MOUNTING. SEE DATA SHEET FOR DETAILS

ORDER PART NUMBER

LT1175CQ
LT1175CQ-5
LT1175IQ
LT1175IQ-5

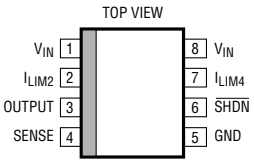


ST PACKAGE
3-LEAD PLASTIC SOT-223

θ_{JA} = 50°C/W WITH BACKPLANE AND 10cm² TOPSIDE LAND SOLDERED TO TAB

ORDER PART NUMBER

LT1175CST-5
LT1175IST-5



S8 PACKAGE
8-LEAD PLASTIC SO

θ_{JA} = 60°C/W TO 100°C/W DEPENDING ON PC BOARD LAYOUT

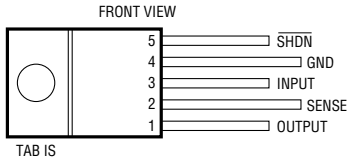
PINS 1, 8 ARE INTERNALLY CONNECTED TO DIE ATTACH PADDLE FOR HEAT SINKING. ELECTRICAL CONTACT CAN BE MADE TO EITHER PIN. FOR BEST THERMAL RESISTANCE, PINS 1, 8 SHOULD BE CONNECTED TO AN EXPANDED LAND THAT IS OVER AN INTERNAL OR BACKSIDE PLANE. SEE APPLICATIONS INFORMATION

ORDER PART NUMBER

LT1175CS8
LT1175CS8-5
LT1175IS8
LT1175IS8-5

S8 PART MARKING

1175 1175I
11755 1175I5



T PACKAGE
5-LEAD PLASTIC TO-220

θ_{JA} = 50°C/W, θ_{JC} = 5°C/W

ORDER PART NUMBER

LT1175CT
LT1175CT-5
LT1175IT
LT1175IT-5

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the operating temperature range, otherwise specifications are at T_A = 25°C. V_{OUT} = 5V, V_{IN} = 7V, I_{OUT} = 0, V_{SHDN} = 3V, I_{LIM2} and I_{LIM4} tied to V_{IN}, T_J = 25°C, unless otherwise noted. To avoid confusion with "min" and "max" as applied to negative voltages, all voltages are shown as absolute values except where polarity is not obvious.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Feedback Sense Voltage	Adjustable Part Fixed 5V Part		3.743 4.93	3.8 5.0	3.857 5.075	V V
Output Voltage Initial Accuracy	Adjustable, Measured at 3.8V Sense Fixed 5V			0.5 0.5	1.5 1.5	% %
Output Voltage Accuracy (All Conditions)	$V_{IN} – V_{OUT}$ = 1V to V_{IN} = 20V, I_{OUT} = 0A to 500mA P = 0 to P_{MAX}, $T_J = T_{MIN}$ to T_{MAX} (Note 3)	●		1.5	2.5	%
Quiescent Input Supply Current	$V_{IN} – V_{OUT} \leq$ 12V	 ●		45	65 80	μA μA

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the operating temperature range, otherwise specifications are at T_A = 25°C. V_{OUT} = 5V, V_{IN} = 7V, I_{OUT} = 0, V_{SHDN} = 3V, I_{LIM2} and I_{LIM4} tied to V_{IN}, T_J = 25°C, unless otherwise noted. To avoid confusion with "min" and "max" as applied to negative voltages, all voltages are shown as absolute values except where polarity is not obvious.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
GND Pin Current Increase with Load (Note 4)		●		10	20	µA/mA
Input Supply Current in Shutdown	V_{SHDN} = 0V			10	20	µA
		●			25	µA
Shutdown Thresholds (Note 9)	Either Polarity On $\overline{SHDN}$ Pin	●	0.8		2.5	V
$\overline{SHDN}$ Pin Current (Note 2)	V_{SHDN} = 0V to 10V (Flows Into Pin)	●		4	8	µA
	V_{SHDN} = –15V to 0V (Flows Into Pin)			1	4	µA
Output Bleed Current in Shutdown (Note 6)	V_{OUT} = 0V, V_{IN} = 15V			0.1	1	µA
		●		1	5	µA
SENSE Pin Input Current	(Adjustable Part Only, Current Flows Out of Pin)	●		75	150	nA
	(Fixed Voltage Only, Current Flows Out of Pin)	●		12	20	µA
Dropout Voltage (Note 7)	I_{OUT} = 25mA	●		0.1	0.2	V
	I_{OUT} = 100mA	●		0.18	0.26	V
	I_{OUT} = 500mA	●		0.5	0.7	V
	I_{LIM2} Open, I_{OUT} = 300mA	●		0.33	0.5	V
	I_{LIM4} Open, I_{OUT} = 200mA	●		0.3	0.45	V
	I_{LIM2}, I_{LIM4} Open, I_{OUT} = 100mA	●		0.26	0.45	V
Current Limit (Note 11)	$V_{IN} – V_{OUT}$ = 1V to 12V	●	520	800	1300	mA
	I_{LIM2} Open	●	390	600	975	mA
	I_{LIM4} Open	●	260	400	650	mA
	I_{LIM2}, I_{LIM4} Open	●	130	200	325	mA
Line Regulation (Note 10)	$V_{IN} – V_{OUT}$ = 1V to V_{IN} = 20V	●		0.003	0.015	%/V
Load Regulation (Note 5, 10)	I_{OUT} = 0mA to 500mA	●		0.1	0.35	%
Thermal Regulation	P = 0 to P_{MAX} (Notes 3, 8) 5-Pin Packages			0.04	0.1	%/W
	8-Pin Packages			0.1	0.2	%/W
Output Voltage Temperature Drift	T_J = 25°C to T_{JMIN}, or 25°C to T_{JMAX}			0.25	1.25	%

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: $\overline{SHDN}$ pin maximum positive voltage is 30V with respect to $–V_{IN}$ and 13.5V with respect to GND. Maximum negative voltage is –20V with respect to GND and –5V with respect to $–V_{IN}$.

Note 3: P_{MAX} = 1.5W for 8-pin packages, and 6W for 5-pin packages. This power level holds only for input-to-output voltages up to 12V, beyond which internal power limiting may reduce power. See Guaranteed Current Limit curve in Typical Performance Characteristics section. Note that all conditions must be met.

Note 4: GND pin current increases because of power transistor base drive. At low input-to-output voltages (< 1V) where the power transistor is in saturation, GND pin current will be slightly higher. See Typical Performance Characteristics.

Note 5: With I_{LOAD} = 0, at T_J > 125°C, power transistor leakage could increase higher than the 10µA to 25µA drawn by the output divider or fixed voltage SENSE pin, causing the output to rise above the regulated value. To prevent this condition, an internal active pull-up will automatically turn on, but supply current will increase.

Note 6: This is the current required to pull the output voltage to within 1V of ground during shutdown.

Note 7: Dropout voltage is measured by setting the input voltage equal to the normal regulated output voltage and measuring the difference between V_{IN} and V_{OUT}. For currents between 100mA and 500mA, with both I_{LIM} pins tied to V_{IN}, maximum dropout can be calculated from V_{DO} = 0.15 + 1.1Ω (I_{OUT}).

Note 8: Thermal regulation is a change in the output voltage caused by die temperature gradients, so it is proportional to chip power dissipation. Temperature gradients reach final value in less than 100ms. Output voltage changes after 100ms are due to absolute die temperature changes and reference voltage temperature coefficient.

Note 9: The lower limit of 0.8V is guaranteed to keep the regulator in shutdown. The upper limit of 2.5V is guaranteed to keep the regulator active. Either polarity may be used, referenced to GND pin.

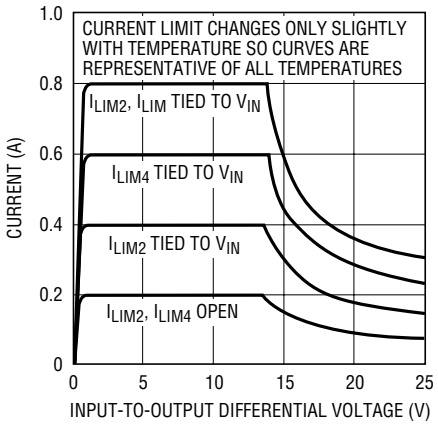
Note 10: Load and line regulation are measured on a pulse basis with pulse width of 20ms or less to keep chip temperature constant. DC regulation will be affected by thermal regulation (Note 8) and chip temperature changes. Load regulation specification also holds for currents up to the specified current limit when I_{LIM2} or I_{LIM4} are left open.

Note 11: Current limit is reduced for input-to-output voltage above 12V. See the graph in Typical Performance Characteristics for guaranteed limits above 12V.

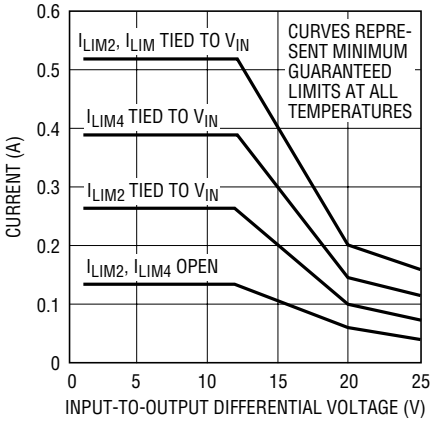
Note 12: Operating at very large input-to-output differential voltages (>15V) with load currents less than 5mA requires an output capacitor with an ESR greater than 1Ω to prevent low level output oscillations.

TYPICAL PERFORMANCE CHARACTERISTICS

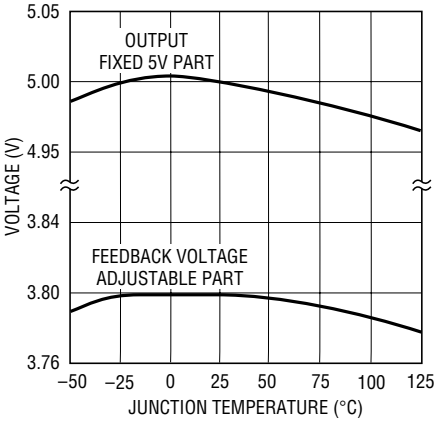
Typical Current Limit Characteristics



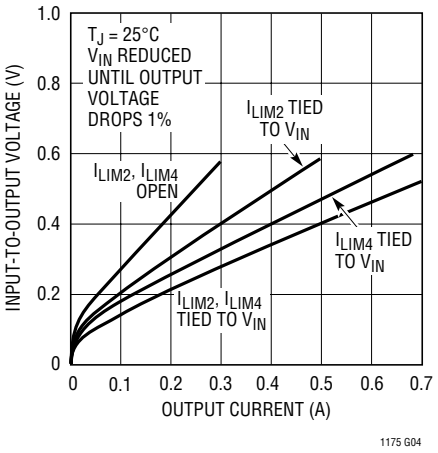
Guaranteed Current Limit



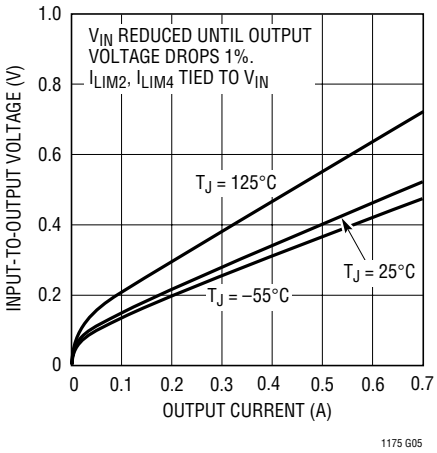
Output Voltage Temperature Drift



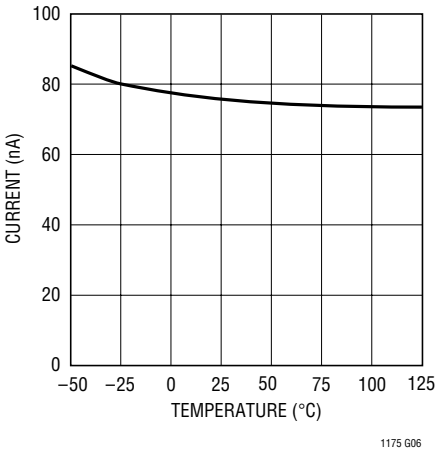
Minimum Input-to-Output Voltage



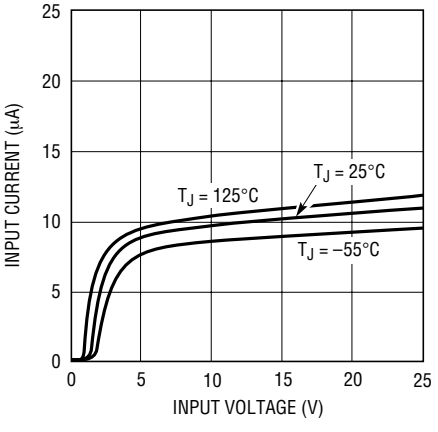
Minimum Input-to-Output Voltage



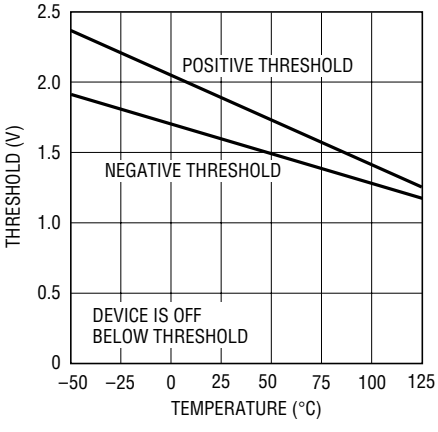
SENSE Bias Current (Adjustable Part)



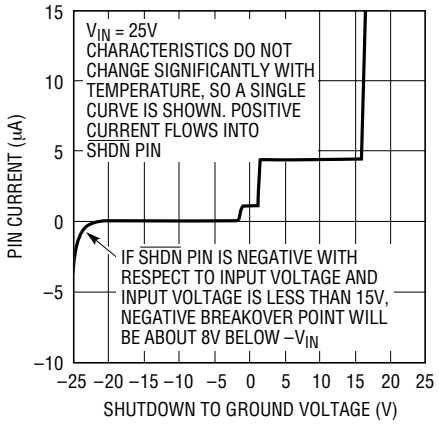
Shutdown Input Current



Shutdown Thresholds

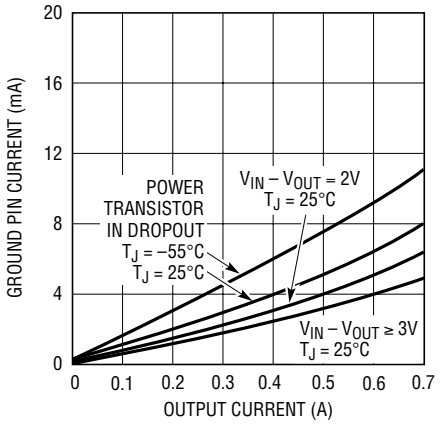


$\overline{\text{SHDN}}$ Pin Characteristics

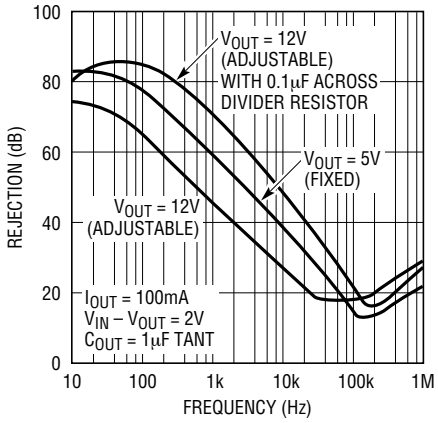


TYPICAL PERFORMANCE CHARACTERISTICS

GND pin Current



Ripple Rejection



RIPPLE REJECTION IS RELATIVELY INDEPENDENT OF INPUT VOLTAGE AND LOAD FOR CURRENTS BETWEEN 25mA AND 500mA. LARGER OUTPUT CAPACITORS DO NOT IMPROVE REJECTION FOR FREQUENCIES BELOW 50kHz. AT VERY LIGHT LOADS, REJECTION WILL IMPROVE WITH LARGER OUTPUT CAPACITORS

PIN FUNCTIONS

SENSE Pin: The SENSE pin is used in the adjustable version to allow custom selection of output voltage, with an external divider set to generate 3.8V at the SENSE pin. Input bias current is typically 75nA flowing out of the pin. Maximum forced voltage on the SENSE pin is 2V and –10V with respect to GND pin.

The fixed 5V version utilizes the SENSE pin to give true Kelvin connections to the load or to drive an external pass transistor for higher output currents. Bias current out of the 5V SENSE pin is approximately 12µA. Separating the SENSE and OUTPUT pins also allows for a new loop compensation technique described in the Applications Information section.

$\overline{\text{SHDN}}$ Pin: The $\overline{\text{SHDN}}$ pin is specially configured to allow it to be driven from either positive voltage logic or with negative only logic. Forcing the $\overline{\text{SHDN}}$ pin 2V either above or below the GND pin will turn the regulator on. This makes it simple to connect directly to positive logic signals for active low shutdown. If no positive voltages are available, the $\overline{\text{SHDN}}$ pin can be driven below the GND pin to turn the regulator on. *When left open, the $\overline{\text{SHDN}}$ pin will default low to a regulator "on" condition.* For all voltages below absolute maximum ratings, the $\overline{\text{SHDN}}$ pin draws only a few microamperes of current (see Typical Performance Characteristics). Maximum voltage on the $\overline{\text{SHDN}}$ pin is 15V, –20V with respect to the GND pin and 35V, –5V with respect to the negative input pin.

I_{LIM} Pins: The two current limit pins are emitter sections of the power transistor. When left open, they float several hundred millivolts above the negative input voltage. When shorted to the input voltage, they increase current limit by a minimum of 200mA for I_{LIM2} and 400mA for I_{LIM4}. These pins must be connected only to the input voltage, either directly or through a resistor.

OUTPUT Pin: The OUTPUT pin is the collector of the NPN power transistor. It can be forced to the input voltage, to ground or up to 2V positive with respect to ground without damage or latchup (see Output Voltage Reversal in Applications Information section). The LT1175 has foldback current limit, so maximum current at the OUTPUT pin is a function of input-to-output voltage. See Typical Performance Characteristics.

GND Pin: The GND pin has a quiescent current of 45µA at zero load current, increasing by approximately 10µA per mA of output current. At 500mA output current, GND pin current is about 5mA. Current flows into the GND pin.

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Note to Reader: To avoid confusion when working with negative voltages (is –6V more or less than –5V?), I have decided to treat the LT1175 as if it were a positive regulator and express all voltages as positive values, both in text and in formulas. If you do the same and simply add a negative sign to the eventual answer, confusion should be avoided. Please don't give me a hard time about "preciseness" or "correctness." I have to field phone calls from around the world and this is my way of dealing with a multitude of conventions. Thanks for your patience.

Setting Output Voltage

The LT1175 adjustable version has a feedback sense voltage of 3.8V with a bias current of approximately 75nA flowing out of the SENSE pin. To avoid output voltage errors caused by this current, the output divider string (see Figure 1) should draw about 25μA. Table 1 shows suggested resistor values for a range of output voltages. The second part of the table shows resistor values which draw only 10μA of current. Output voltage error caused by bias current with the lower valued resistors is about 0.4% maximum and with the higher values, about 1% maximum. A formula is also shown for calculating the resistors for any output voltage.

Table 1

OUTPUT VOLTAGE	R1 I_{DIV} = 25μA	R2 NEAREST 1%	R1 I_{DIV} = 10μA	R2 NEAREST 1%
5V	150k	47.5k	383k	121k
6V	150k	86.6k	383k	221k
8V	150k	165k	383k	422k
10V	150k	243k	383k	619k
12V	150k	324k	383k	825k
15V	150k	442k	383k	1.13M

$$R1 = \frac{3.8V}{I_{DIV}}$$

$$R2 = \frac{R1\left(V_{OUT} - 3.8V\right)}{3.8V} \quad \left(\text{Simple formula}\right)$$

$$R2 = \frac{R1\left(V_{OUT} - 3.8V\right)}{3.8V + R1\left(I_{FB}\right)} \quad \left(\begin{array}{l}\text{Taking SENSE pin bias}\\ \text{current into account}\end{array}\right)$$

I_{DIV} = Desired divider current

The LT1175-5 is a fixed 5V design with the SENSE pin acting as a Kelvin connection to the output. Normally the SENSE pin and the OUTPUT pin are connected directly together, either close to the regulator or at the remote load point.

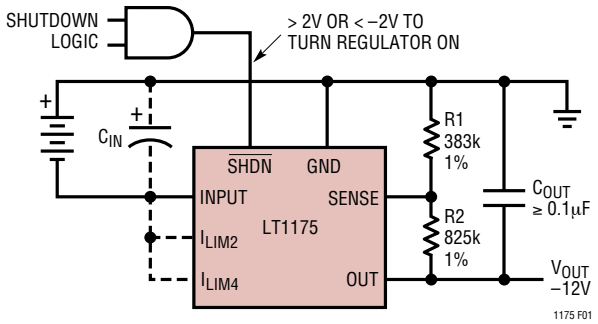


Figure 1. Typical LT1175 Adjustable Connection

Setting Current Limit

The LT1175 uses two I_{LIM} pins to set current limit (typical) at 200mA, 400mA, 600mA or 800mA. The corresponding minimum guaranteed currents are 130mA, 260mA, 390mA and 520mA. This allows the user to select a current limit tailored to his specific application and prevents the situation where short-circuit current is many times higher than full-load current. Problems with input supply overload or excessive power dissipation in a faulted load are prevented. Power limiting in the form of foldback current limit is built in and reduces current limit as a function of input-to-output voltage differential for differentials exceeding 14V. See the graph in Typical Performance Characteristics. The LT1175 is guaranteed to be blowout-proof regardless of current limit setting. The power limiting combined with thermal shutdown protects the device from destructive junction temperatures under all load conditions.

Shutdown

In shutdown, the LT1175 draws only about 10μA. Special circuitry is used to minimize increases in shutdown current at high temperatures, but a slight increase is seen above 125°C. One option *not taken* was to actively pull down on the output during shutdown. This means that the output will fall slowly after shutdown is initiated, at a rate determined by load current plus the 12μA internal load, and the size of the output capacitor. Active pull-down is

APPLICATIONS INFORMATION

normally a good thing when the regulator is used by itself, but it prevents the user from shutting down the regulator when a second power source is connected to the LT1175 output. If active output pull-down is needed in shutdown, it can be added externally with a depletion mode PFET as shown in Figure 2. Note that the maximum pinch-off voltage of the PFET must be less than the positive logic high level to ensure that the device is completely off when the regulator is active. The Motorola J177 device has 300Ω on resistance for zero gate source voltage.

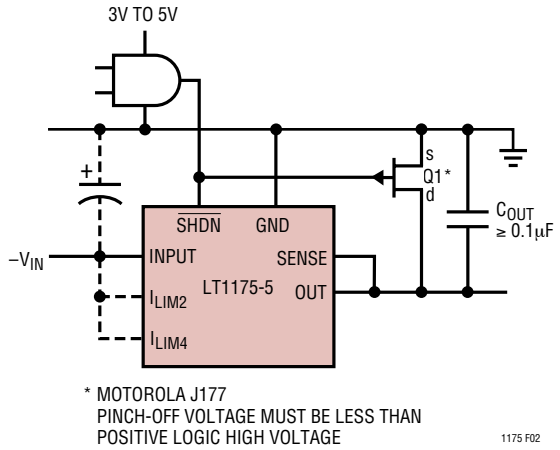


Figure 2. Active Output Pull-Down During Shutdown

Minimum Dropout Voltage

Dropout voltage is the minimum voltage required between input and output to maintain proper output regulation. For older 3-terminal regulator designs, dropout voltage was typically 1.5V to 3V. The LT1175 uses a saturating power transistor design which gives much lower dropout voltage, typically 100mV at light loads and 450mV at full load. Special precautions were taken to ensure that this technique does not cause quiescent supply current to be high under light load conditions. When the regulator input voltage is too low to maintain a regulated output, the pass transistor is driven hard by the error amplifier as it tries to maintain regulation. The current drawn by the driver transistor could be tens of milliamperes even with little or no load on the output. This indeed was the case for older IC designs that did not actively limit driver current when the power transistor saturated. The LT1175 uses a new antisaturation technique that prevents high driver current, yet allows the power transistor to approach its theoretical saturation limit.

Output Capacitor

Several new regulator design techniques are used to make the LT1175 extremely tolerant of output capacitor selection. Like most low dropout designs which use a collector or drain of the power transistor to drive the output node, the LT1175 uses the output capacitor as part of the overall loop compensation. Older regulators generally required the output capacitor to have a minimum value of 1µF to 100µF, a *maximum* ESR (Effective Series Resistance) of 0.1Ω to 1Ω and a *minimum* ESR in the range of 0.03Ω to 0.3Ω. These restrictions usually could be met only with good quality solid tantalum capacitors. Aluminum capacitors have problems with high ESR unless much higher values of capacitance are used (physically large). The ESR of ceramic or film capacitors was too *low*, which made the capacitance/ESR zero frequency too high to maintain phase margin in the regulator. Even with optimum capacitors, loop phase margin was very low in previous designs when output current was low. These problems led to a new design technique for the LT1175 error amplifier and internal frequency compensation as shown in Figure 3.

A conventional regulator loop consists of error amplifier A1, driver transistor Q2 and power transistor Q1. Added to this basic loop are secondary loops generated by Q3 and C_F. A DC negative feedback current fed into the error amplifier through Q3 and R_N causes overall loop current gain to be very low at light load currents. This is not a problem because very little gain is needed at light loads. In addition to low gain, the parasitic pole frequency at Q2 base is extended by the DC feedback. The combination of these two effects dramatically improves loop phase margin at light loads and makes the loop tolerant of large ESR in the output capacitor. With heavy loads, loop phase and gain are not nearly as troublesome and large negative feedback could degrade regulation. The logarithmic behavior of the base emitter voltage of Q1 reduces Q3 negative feedback at heavy loads to prevent poor regulation.

In a conventional design, even with the nonlinear feedback, poor loop phase margin would occur at medium to heavy loads if the ESR of the output capacitor fell below

APPLICATIONS INFORMATION

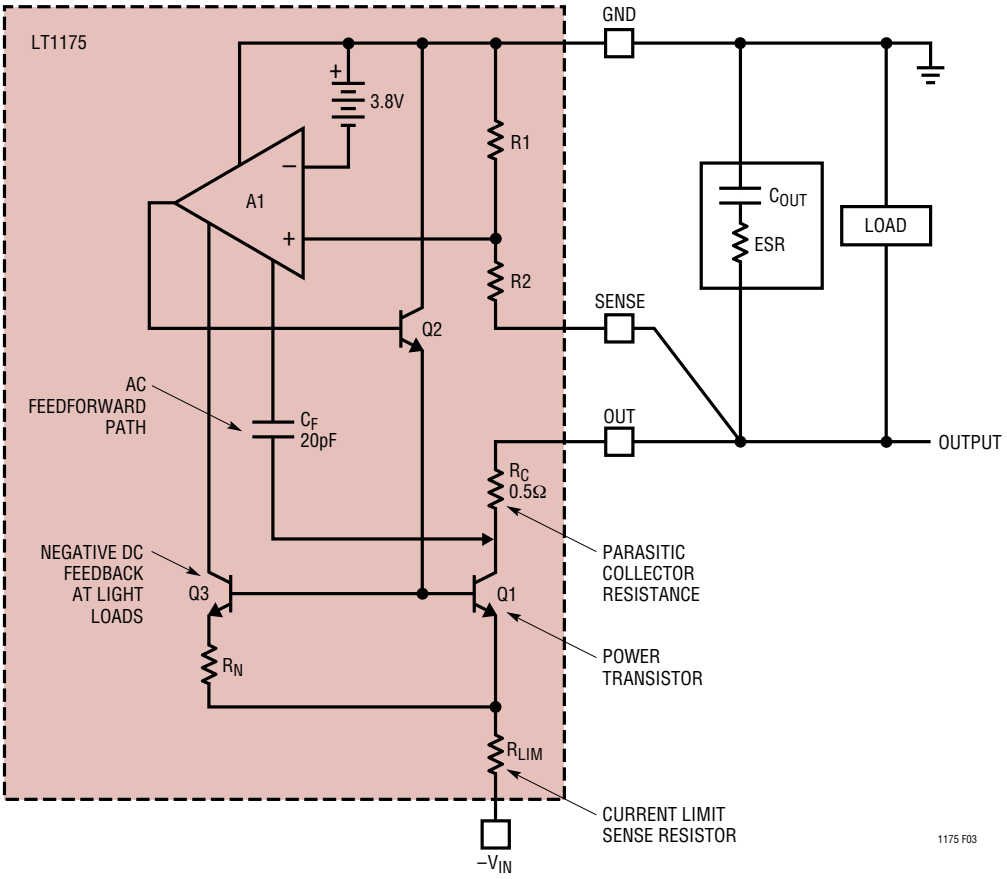


Figure 3

0.3Ω. This condition can occur with ceramic or film capacitors which often have an ESR under 0.1Ω. With previous designs, the user was forced to add a real resistor in series with the capacitor to guarantee loop stability. The LT1175 uses a unique AC feedforward technique to eliminate this problem. C_F is a conventional feedforward capacitor often used in regulators to cancel the pole formed by the output capacitor. It would normally be connected from the regulated output node to the feedback node at the R1/R2 junction or to an internal node on the amplifier as shown. In this case, however, the capacitor is connected to the internal structure of the power transistor. R_C is the unavoidable parasitic collector resistance of the power transistor. Access to the node at the bottom of R_C is available only in monolithic structures where Kelvin connections can be made to the NPN buried collector layer. The loop now responds as if R_C were in series with the output capacitor and good loop stability is achieved even with extremely low ESR in the output capacitor.

The end result of all this attention to loop stability is that the output capacitor used with the LT1175 can range in value from 0.1μF to hundreds of microfarads, with an ESR from 0Ω to 10Ω. This range allows the use of ceramic, solid tantalum, aluminum and film capacitors over a wide range of values.

The optimum output capacitor type for the LT1175 is still solid tantalum, but there is considerable leeway in selecting the exact unit. If large load current transients are expected, larger capacitors with lower ESR may be needed to control worst-case output variation during transients. If transients are not an issue, the capacitor can be chosen for small physical size, low price, etc. Concerns about surge currents in tantalum capacitors are not an issue for the output capacitor because the LT1175 limits inrush current to well below the level which can cause capacitor damage. Surges caused by shorting the regulator output are also not a problem because tantalum capacitors do not fail

APPLICATIONS INFORMATION

during a "shorting out" surge, only during a "charge up" surge.

The output capacitor should be located within several inches of the regulator. If remote sensing is used, the output capacitor can be located at the remote sense node, but the GND pin of the regulator should also be connected to the remote site. The basic rule is to keep SENSE and GND pins close to the output capacitor, regardless of where it is.

Operating at very large input-to-output differential voltages (>5V) with load currents less than 5mA requires an output capacitor with an ESR greater than 1Ω to prevent low level output oscillations.

Input Capacitor

The LT1175 requires a separate input bypass capacitor only if the regulator is located more than six inches from the raw supply output capacitor. A 1μF or larger tantalum capacitor is suggested for all applications, but if low ESR capacitors such as ceramic or film are used for the output *and* input capacitors, the input capacitor should be at least three times the value of the output capacitor. If a solid tantalum or aluminum electrolytic output capacitor is used, the input capacitor is very noncritical.

High Temperature Operation

The LT1175 is a micropower design with only 45μA quiescent current. This could make it perform poorly at high temperatures (>125°C), where power transistor leakage might exceed the output node loading current (5μA to 15μA). To avoid a condition where the output voltage drifts uncontrolled high during a high temperature no-load condition, the LT1175 has an active load which turns on when the output is pulled above the nominal regulated voltage. This load absorbs power transistor leakage and maintains good regulation. There is one downside to this feature, however. If the output is pulled high deliberately, as it might be when the LT1175 is used as a backup to a slightly higher output from a primary regulator, the LT1175 will act as an unwanted load on the primary regulator. Because of this, the active pull-down is deliberately "weak." It can be modeled as a 2k resistor in series with an internal clamp voltage when the regulator output is being pulled high. If a 4.8V output is pulled to 5V, for instance, the load on the primary regulator would be (5V – 4.8V)/2kΩ = 100μA. This also means that if the internal pass transistor leaks 50μA, the output voltage will be (50μA)(2kΩ) = 100mV high. This condition will not occur under normal operating conditions, but could occur immediately after an output short circuit had overheated the chip.

Thermal Considerations

The LT1175 is available in a special 8-pin surface mount package which has Pins 1 and 8 connected to the die attach paddle. This reduces thermal resistance when Pins 1 and 8 are connected to expanded copper lands on the PC board. Table 2 shows thermal resistance for various combinations of copper lands and backside or internal planes. Table 2 also shows thermal resistance for the 5-pin DD surface mount package and the 8-pin DIP and package.

Table 2. Package Thermal Resistance (°C/W)

LAND AREA	DIP	ST	SO	Q
Minimum	140	90	100	60
Minimum with Backplane	110	70	80	50
1cm^2 Top Plane with Backplane	100	64	75	35
10cm^2 Top Plane with Backplane	80	50	60	27

To calculate die temperature, maximum power dissipation or maximum input voltage, use the following formulas with correct thermal resistance numbers from Table 2. For through-hole TO-220 applications use θ_{JA} = 50°C/W without a heat sink and θ_{JA} = 5°C/W + heat sink thermal resistance when using a heat sink.

$$\text{Die Temp} = T_A + \theta_{JA}\left(V_{IN} - V_{OUT}\right)\left(I_{LOAD}\right)$$

$$\text{Maximum Power Dissipation} = \frac{T_{MAX} - T_A}{\theta_{JA}}$$

$$\text{Maximum Input Voltage for Thermal Considerations} = \frac{T_{MAX} - T_A}{\theta_{JA}\left(I_{LOAD}\right)} + V_{OUT}$$

APPLICATIONS INFORMATION

T_A = Maximum ambient temperature

T_{MAX} = Maximum LT1175 die temperature (125°C for commercial and industrial grades)

θ_{JA} = LT1175 thermal resistance, junction to ambient

V_{IN} = Maximum continuous input voltage at maximum load current

I_{LOAD} = Maximum load current

Example: LT1175S8 with I_{LOAD} = 200mA, V_{OUT} = 5V, V_{IN} = 7V, T_A = 60°C. Maximum die temperature for the LT1175S8 is 125°C. Thermal resistance from Table 2 is found to be 80°C/W.

Die Temperature = 60 + 80 (0.2A)(8 – 5) = 108°C

$$\text{Maximum Power Dissipation} = \frac{125-60}{80} = 0.81\text{W}$$

$$\text{Maximum Continuous Input Voltage (for Thermal Considerations)} = \frac{125-60}{80(0.2)} + 5 = 9\text{V}$$

Output Voltage Reversal

The LT1175 is designed to tolerate an output voltage reversal of up to 2V. Reversal might occur, for instance, if the output was shorted to a positive 5V supply. This would almost surely destroy IC devices connected to the negative output. Reversal could also occur during start-up if the positive supply came up first and loads were connected between the positive and negative supplies. *For these reasons, it is always good design practice to add a reverse biased diode from each regulator output to ground to limit output voltage reversal*. The diode should be rated to handle full negative load current for start-up situations, or the short-circuit current of the positive supply if supply-to-supply shorts must be tolerated.

Input Voltage Lower Than Output

Linear Technology's positive low dropout regulators LT1121 and LT1129, will not draw large currents if the input voltage is less than the output. These devices use a lateral PNP power transistor structure that has 40V emitter base breakdown voltage. *The LT1175, however, uses an NPN power transistor structure that has a parasitic diode between the input and output of the regulator*. Reverse voltages between input and output above 1V will damage the regulator if large currents are allowed to flow. Simply disconnecting the input source with the output held up will not cause damage even though the input-to-output voltage will become slightly reversed.

High Frequency Ripple Rejection

The LT1175 will sometimes be powered from switching regulators that generate the unregulated or quasi-regulated input voltage. This voltage will contain high frequency ripple that must be rejected by the linear regulator. Special care was taken with the LT1175 to maximize high frequency ripple rejection, but as with any micropower design, rejection is strongly affected by ripple frequency. The graph in the Typical Performance Characteristics section shows 60dB rejection at 1kHz, but only 15dB rejection at 100kHz for the 5V part. Photographs in Figures 4a and 4b show actual output ripple waveforms with square wave and triwave input ripple.

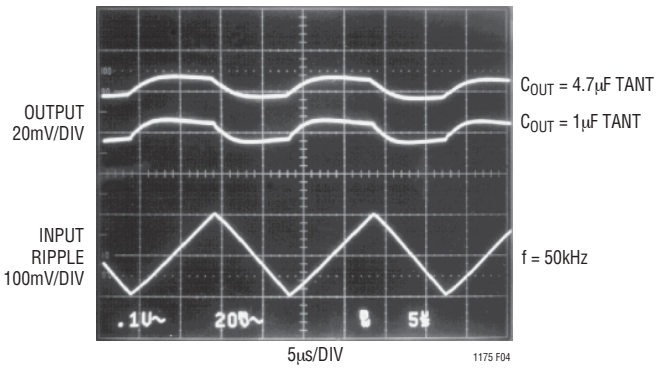


Figure 4a.

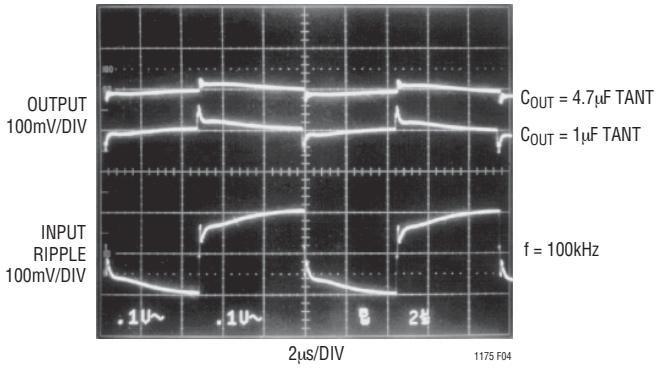


Figure 4b.

APPLICATIONS INFORMATION

To estimate regulator output ripple under different conditions, the following general comments should be helpful:

1. Output ripple at high frequency is only weakly affected by load current or output capacitor size for medium to heavy loads. At very light loads (<10mA), higher frequency ripple may be reduced by using larger output capacitors.
2. A feedforward capacitor across the resistor divider used with the adjustable part is effective in reducing ripple only for output voltages greater than 5V and only for frequencies less than 100kHz.
3. Input-to-output voltage differential has little effect on ripple rejection until the regulator actually enters a dropout condition of 0.2V to 0.6V.

If ripple rejection needs to be improved, an input filter can be added. This filter can be a simple RC filter using a 1Ω to 10Ω resistor. A 3.3Ω resistor for instance, combined with a 0.3Ω ESR solid tantalum capacitor, will give an additional 20dB ripple rejection. The size of the resistor will be dictated by maximum load current. If the maximum voltage drop allowable across the resistor is "V_R," and maximum load current is I_{LOAD}, $R = V_R/I_{LOAD}$. At light loads, larger resistors and smaller capacitors can be used to save space. At heavier loads an inductor may have to be used in place of the resistor. The value of the inductor can be calculated from:

$$L_{FIL} = \frac{ESR}{2\pi(f)\left(10^{rr/20}\right)}$$

ESR = Effective series resistance of filter capacitor. This assumes that the capacitive reactance is small compared to ESR, a reasonable assumption for solid tantalum capacitors above 2.2μF and 50kHz.

f = Ripple frequency

rr = Ripple rejection ratio of filter in dB

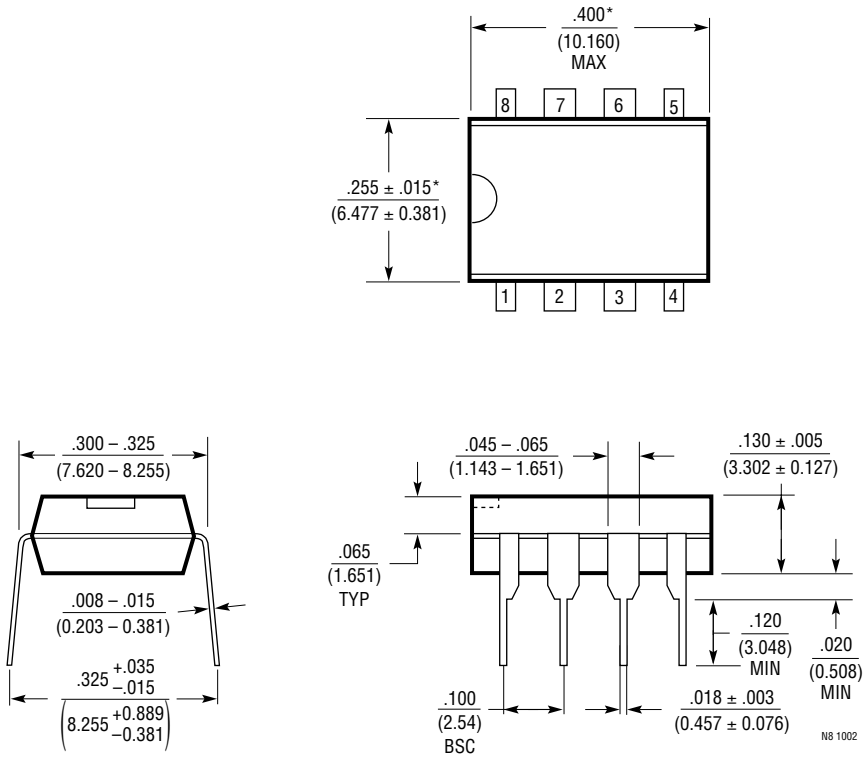
Example: ESR = 1.2Ω, f = 100kHz, rr = –25dB.

$$L_{FIL} = \frac{1.2}{6.3\left(10^{5}\right)\left(10^{-25/20}\right)} = 34\mu H$$

Solid tantalum capacitors are suggested for the filter to keep filter Q fairly low. This prevents unwanted ringing at the resonant frequency of the filter and oscillation problems with the filter/regulator combination.

PACKAGE DESCRIPTION

N8 Package
8-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510)

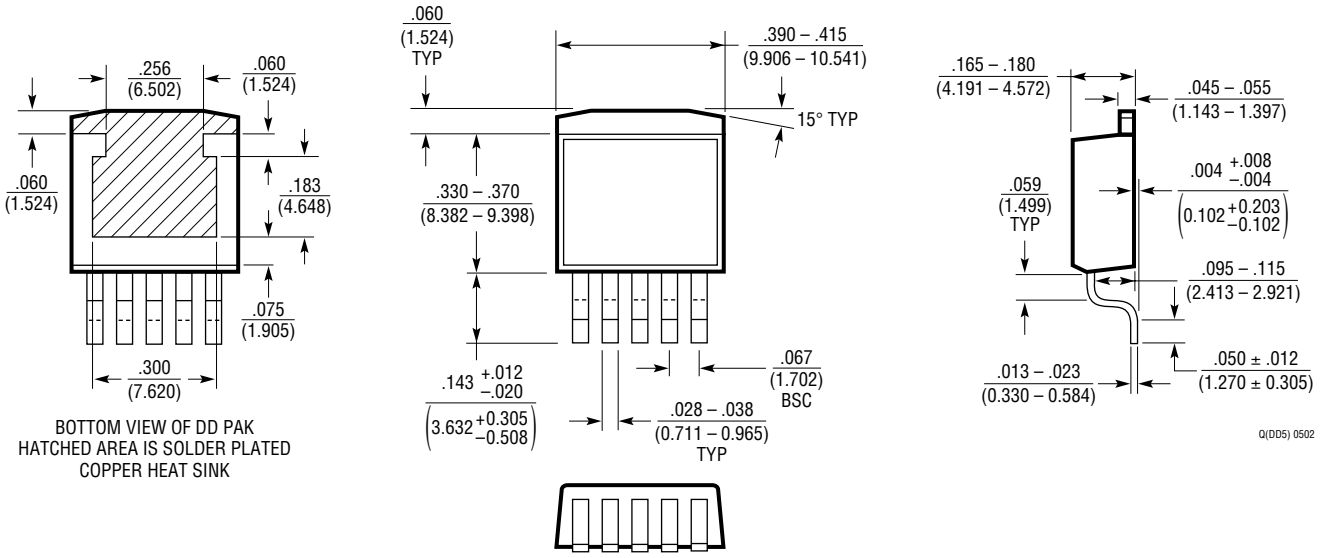


NOTE:
1. DIMENSIONS ARE $\frac{\text{INCHES}}{\text{MILLIMETERS}}$

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

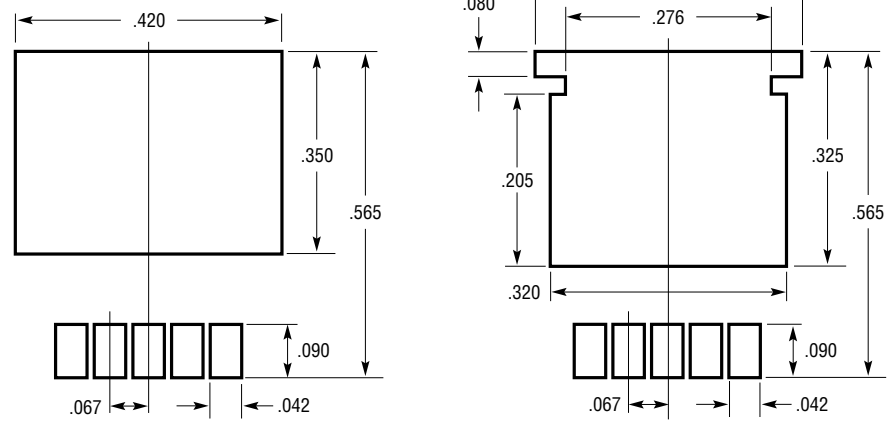
PACKAGE DESCRIPTION

Q Package
5-Lead Plastic DD Pak
(Reference LTC DWG # 05-08-1461)



BOTTOM VIEW OF DD PAK
HATCHED AREA IS SOLDER PLATED
COPPER HEAT SINK

Q(DD5) 0502



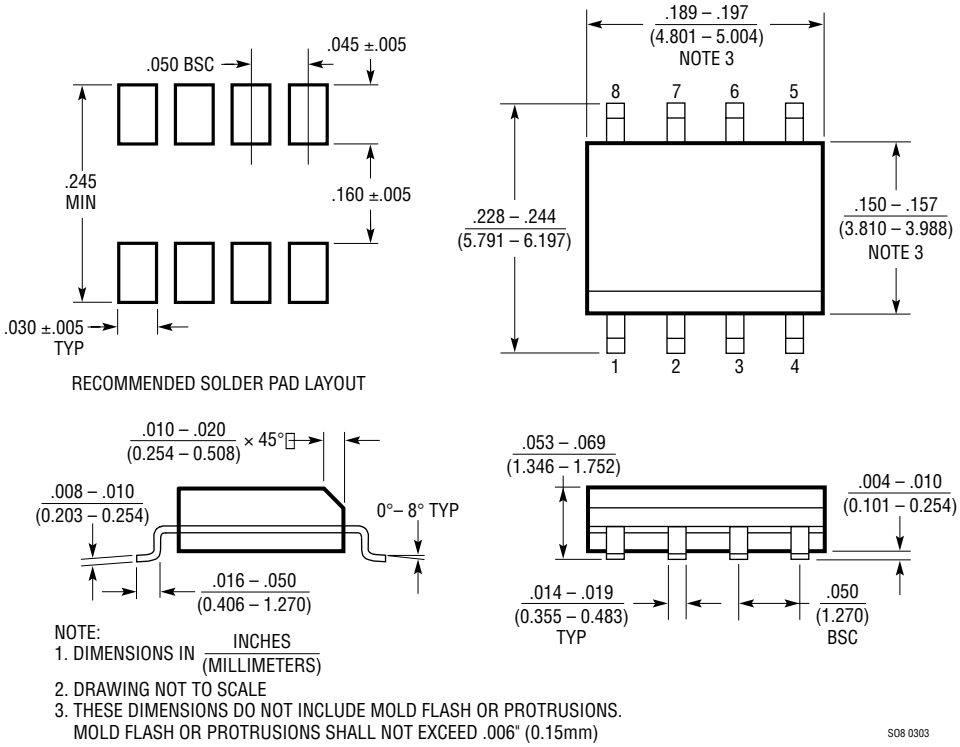
RECOMMENDED SOLDER PAD LAYOUT

RECOMMENDED SOLDER PAD LAYOUT
FOR THICKER SOLDER PASTE APPLICATIONS

NOTE:
1. DIMENSIONS IN INCH/(MILLIMETER)
2. DRAWING NOT TO SCALE

PACKAGE DESCRIPTION

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)

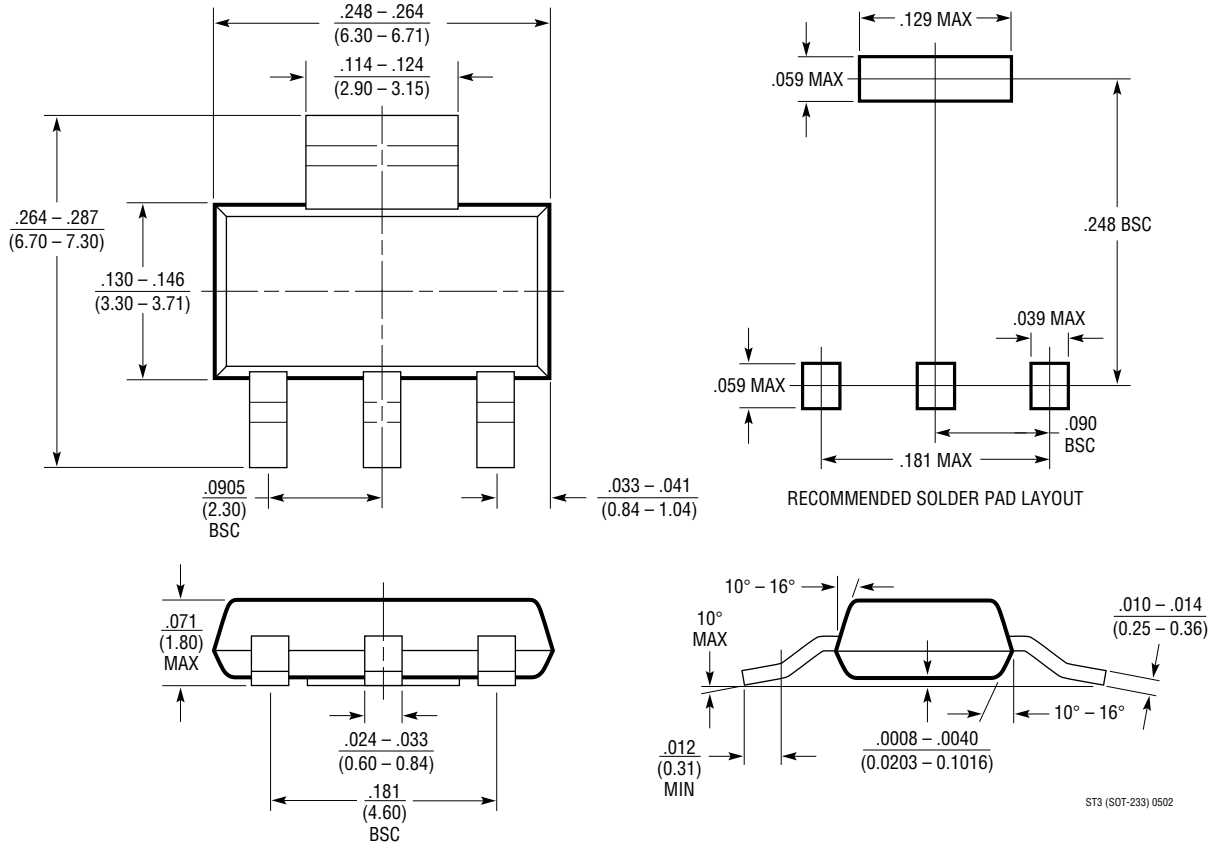


NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

SO8 0303

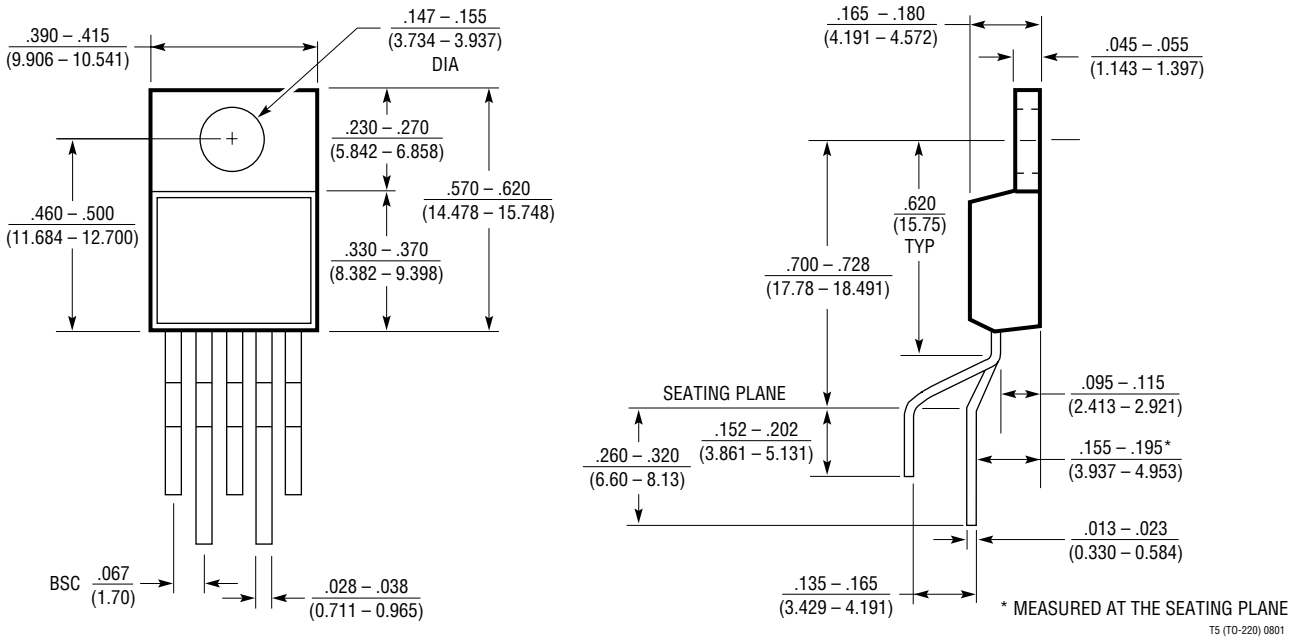
PACKAGE DESCRIPTION

ST Package
3-Lead Plastic SOT-223
(Reference LTC DWG # 05-08-1630)



PACKAGE DESCRIPTION

T Package
5-Lead Plastic TO-220 (Standard)
(Reference LTC DWG # 05-08-1421)



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1121	150mA Positive Micropower Low Dropout Regulator with Shutdown	
LT1129	700mA Positive Micropower Low Dropout Regulator with Shutdown	
LT1185	3A Negative Low Dropout Regulator	
LT1521	300mA Positive Micropower Low Dropout Regulator with Shutdown	
LT1529	3A Positive Micropower Low Dropout Regulator with Shutdown	

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